07/680,747

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EXAMINER
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ART UNIT	PAPER NUMBER
2502	5

DATE MAILED: 12/21/92

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-17 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-17 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☒ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☒ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

1) This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

See PTO form 948.

2) Claims **1-5,16-17** are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) The phrase including " *imperfectly isolating* " (claims 1, 16) is unclear and cannot be understood. What is the meaning of this phrase ?

b) Claims 2-5 and 17 incorporate the unclear of claims 1 and 16 by virtue of their dependency thereon.

3) The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

4) (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5) (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6) Claims **1-17** are rejected under 35 U.S.C. § 102(b) as being *clearly anticipated* by **CHEN Y. WANG (4,991,142)**.

a) WANG discloses a dynamic random access memory (DRAM) as claimed in claims *1,6,7,10* and *16*, comprising :

a plurality of bit storage capacitors (column 1, lines 10-17);

a folded bit line comprises of a complementary pair bit lines (Fig.1, Bit lines in row);

a sense amplifier (Fig.1, 26,28);

means connecting bit line to sense nodes for imperfectly isolating sense nodes from the bit line (Fig.1, Isolators 14, Isolator control *ϕ3*);

means for enabling sense amplifier (Fig.1, *ϕ5, ϕ6*);

means for disabling isolating means (Fig.1, *ϕ3*);

power supply means for providing full high and full low logic level voltage (Fig.1, Vss, Vcc);

a pair of field effect transistors connected to power supply, and means for providing restore and sense signals to gates of these FETs (Fig.1, FET 34, FET 32, *ϕ6, ϕ5*).

b) As to claims *2,4* and *17*, WANG shows isolating means including a pair of field effect transistors (Fig.1, 14).

c) As to claims *3* and *5*, WANG shows disabling means comprises a voltage source (ϕ3).

d) As to claims *8,9,14,15*, WANG shows sense amplifier in figure 1, RT1, RT2, SA3, SA4 FETS 34,32 and *ϕ6, ϕ5*).

e) As to claims *11-13*, WANG shows DRAM comprises a

plurality of bit lines and associated with sense amplifiers (see figure 1, Bit Lines 10, 12).

7) Claims **1-17** are further rejected under 35 U.S.C. § 102(b) as being anticipated by **MIYAMOTO et al (4,780,850** and **4,803,663)**.

MIYAMOTO et al discloses a DRAM as claimed in claims 1-17 (see **4,780,850** figure 12, *Isolators Q14, Q15; Isolator control TR; Sense Amplifier Q1a, Q2a, Q3a, Q4a; Power Sources Vcc, Vss; FETs QSNa, QSPa; Enabling Signals SNa, SPa;* and **4,803,663**, figure 1, *Isolators QT3, QT4; Sense Amplifier SA; Power Source Vcc, Vss; FETs QN5, QP5; Enabling Signals SN, SP1*).

8) The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

MIYATAKE (5,020,031) discloses a dynamic random access memory (DRAM) including isolator FETs, isolator control signals, sense amplifier, sense amplifier control signals and a power source for providing a full high (Vcc) and a full low (Vss) of power supply.

SUWA et al (4,833,654) discloses a dynamic random access memory (DRAM) including isolator FETs, isolator control signals, sense amplifier, sense amplifier control signals and a power source for providing a full high (Vcc) and a full low (Vss) of power supply.

WADA et al (4,941,128) discloses a dynamic random access

memory (DRAM) including isolator FETs, isolator control signals, sense amplifier, sense amplifier control signals and a power source for providing a full high (Vcc) and a full low (Vss) of power supply.

KOMATSU et al (4,943,960) discloses a dynamic random access memory (DRAM) including isolator FETs, isolator control signals, sense amplifier, sense amplifier control signals and a power source for providing a full high (Vcc) and a full low (Vss) of power supply.

9) Any inquiry concerning this communication or earlier communications from the examiner should be directed to **TAN DINH** whose telephone number is (703) 308-4859.

Any inquiry of a general nature or relating to the status of this application should be directed to ***the Group receptionist*** whose telephone number is (703) 308-0956.

ROBERT J. PASCAL
PRIMARY EXAMINER
ART UNIT 252

T.D
December 19, 1992